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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,983	02/25/2005	Isami Kato	5000-5247	5011
27123	7590	10/09/2007		
MORGAN & FINNEGAN, L.L.P. 3 WORLD FINANCIAL CENTER NEW YORK, NY 10281-2101			EXAMINER KINKEAD, ARNOLD M	
			ART UNIT	PAPER NUMBER
			2817	
			NOTIFICATION DATE	DELIVERY MODE
			10/09/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary

Application No.

10/525,983

Applicant(s)

KATO ET AL.

Examiner

Arnold Kinhead

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 July 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____

- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCorquodale et al in view of Gupta(US 6,362,698) and Mucke et al(US 6,268,778) all of record and further in view of Weldon et al (IEEE, ISSCC 12/2001 new cite)
The reference to McCorquodale et al discloses **an integrated VCO that is may be formed on an IC with a divider output to a mixer for the RF stage...(see background for various implementations)**, see figures 7C, and 8A, the oscillator circuit (see figure 7C)comprising an inductor(72) coupled between the cross-coupled

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MOSFET transistors (with gates of respective MOSFETs being coupled to either the source or drain of the other MOSFET in the cross coupled config); a divider, square wave periodic (50% duty inherent), is shown in figure 8A which divides the output of the VCO (f/n); these elements are formed on the same semiconductor (see col. 13, lines 40-57.) A variable capacitor is shown (52') as part of the tuning circuit controlled by a control signal (V_{ctrl}) developed in the PLL. In the summary, and figure 8A/b, **the use of the integrated VCO and divider is highlighted, see col. 13, lines 22-45. The divider representing an "external loop" divider. Please note that examiner believes the Q and Qbar outputs represent the two 180 degree phase shifted signals, albeit one being feedback.**

The reference does not show several conventional and equivalent details such as the use of equivalent MOSFET devices (MOSCAPs) instead of the MEMs integrated capacitors for varying frequency of the vco, nor the details of the PLL system which includes the LPF, phase detector, and charge pump for generating the DC control voltage to control the VCO. Also, no representation of the output signal being supplied to a mixer.

With regards the PLL system, the reference by Gupta highlights the prior art PLL system, see figure 1, which shows, phase detector (12), pump (14), LPF (16) for developing the dc error control for the VCO (18) and divider (programmable (N), counter/divider 22). Again this is conventional and allows VCO control to a target frequency. With regards the use of MOSCAPs, MOSFET devices coupled to be equivalent variable capacitors, the reference by Mucke et al, see figure 2, and col. 8,

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lines 49-end of column which highlight the use of integrated type capacitance elements that are formed by MOSFETs. Again this is equivalent to the variable caps described by McCorquodale et al. for tuning a VCO.

The above references do not show use of the divided output being sent to a mixer, for example, as a LO input. The reference to Weldon et al is relied on, see figure 10.4.1 and external divider element supplying phased outputs to a mixer for the required conversion.

In light of the above it would have been obvious for one of ordinary skill in the art to have used the equivalent MOSCAP capacitances as noted in Mucke et al for the integrated caps shown by McCorquodale et al; these being functionally equivalent capacitors that allow for integration. The conventional PLL structure is highlighted in the Gupta reference and could be used to incorporate the VCO and external divider as highlighted in McCorquodale et al for full integration. The use of a phased output with desired frequency division for use as a LO signal input in transceivers being shown in general by the Weldon et al reference.

Response to Arguments

Applicant's arguments filed 07-23-07 have been fully considered but they are not persuasive. The examiner has considered the arguments and maintains the references as applied; Firstly, the Weldon reference is relied on to show that the PLL may be used to supply an external divider for bringing the frequency in line for use as a LO signal as desired.

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The use of internal and external PLL loop dividers is conventional and as shown by the references above, enhance the frequency as desired for the system overall. The secondary references serve to highlight conventional MOSCAPs, divider applications and integration of these in communication systems overall.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arnold M. Kinkead whose telephone number is 571-272-1763. The examiner can normally be reached on Mon-Fri, 8:30 am -5 pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Arnold M Kinhead
Primary Examiner
Art Unit 2817

Arnold Kinhead
09-30-07